

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S107	620	((logic near design) and (layout near design) and @ad<"20031128"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:08
S108	230	((logic near design) and ((layout physical) near design) and @ad<"20031128" and ((allocat\$5 floorplan\$5 (floor adj plan\$5) insert\$3) with (clock\$3 clk delay buffer driver repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:17
S109	18	@ad<"20031128" and (optim\$7 verif\$7 correct\$3 fix\$4) near5 (timing time clock\$3 delay skew) with ((before prior\$2 preced\$4) near3 (layout))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/07 20:26
S113	2523	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design \$3 process\$3 routine))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:39
S115	421	@ad<"20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:42

S114	1856	@ad< "20031128" and delay and skew and ((logic circuit functional (front near2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back near2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:42
S116	421	@ad< "20031128" and delay and skew and ((logic circuit functional (front adj2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back adj2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:43
S117	230	@ad< "20031128" and delay and skew and ((logic circuit functional (front adj2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back adj2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient spice) near3 (analy\$7))) and (cts (clock near3 tree) (allocat\$4 near4 (clock clk buffer driver)) ((clock clk tree) near2 build\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:45
S118	76	@ad< "20031128" and delay and skew and ((logic circuit functional (front adj2 end)) with (phase stage design\$3 process\$3 routine)) and ((physical layout (back adj2 end)) with (phase stage design \$3 process\$3 routine)) and ((number value) with (clock tree buffer driver repeater)) and (sta or ((time timing transient	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 01:46

		spice) near3 (analy\$7))) and (cts (clock near3 tree) (allocat\$4 near4 (clock clk buffer driver)) ((clock clk tree) near2 build\$3)) and "716".clas.				
S119	2701	@ad<"20031128" and (timing netlist sta (logic near (design phase stage))) with (verif\$7 optim \$7 test\$3 check\$4 fix\$4 correct\$5) and (layout with (verif\$5 optim\$7 test\$3 check\$4 fix\$4 correct\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:17
S120	238	@ad<"20031128" And ((technology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) netlist (logic\$2 near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And ((technology near dependent) (back adj end) layout (physical near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And (clock timing buffer) with (spec specification configuration requirement definition defin\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:23
S121	206	@ad<"20031128" And ((technology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) netlist (logic\$2 near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And ((technology near dependent) (back adj end) layout (physical near2 (phase stage design\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:24

		process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And (clock timing buffer) with (spec specification configuration requirement definition defin\$3) and "716".clas.				
S122	161	@ad<"20031128" And ((technology near independent) (front adj end) functional rtl hdl ((gate near level) near (specification description)) netlist (logic\$2 near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And ((technology near dependent) (back adj end) layout (physical near2 (phase stage design\$3 process\$3 routine))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice) And (clock timing buffer) with (spec specification definition defin\$3) and "716".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:27
S123	1	@ad<"20031128" And (netlist near5 ((gate near level) rtl functional logic \$2)) with ((timing near5 (analy\$5 closure converg \$5 verif\$5 optim\$7 check \$4 static validat\$3)) sta spice) And ((time timing timed) near3 (driv\$3) near3 layout)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 14:47

S126	4233	@ad<"20031128" And ((netlist near5 ((gate near level) rtl verilog vhdl functional logic\$2)) (gate adj level) (logic\$2 adj (stage phase design routine)) ((clock buffer) with (skeleton synthesis tree))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice)) And (layout same ((timing near5 (analy \$5 closure converg\$5 verif \$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And (clock timing buffer) with (spec specification configuration requirement definition defin \$3 character\$7 constraint goal) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5) with (clock near (net source domain structure element block need\$4 used utiliz\$7)) And (clock buffer) with (allocat \$4 defin\$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:06
S127	72	@ad<"20031128" And (netlist (((gate adj level) netlist rtl hdl verilog vhdl logic\$2) adj (stage phase design routine)) ((clock buffer) near4 (skeleton synthesis tree)) ((clock buffer) near2 (tree distribution) near2 synthes \$7)) with ((timing near5 (analy\$5 closure converg \$5 verif\$5 optim\$7 check \$4 static validat\$3)) sta spice)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) with (spec specification configuration requirement definition defin \$3 character\$7 constraint	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:12

		goal) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list\$3 report \$3) with (clock near (net source domain structure element block need\$4 used utiliz\$7))) And (clock buffer) with (allocat\$4 defin \$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5)				
S128	72	@ad<"20031128" And (netlist (((gate adj level) netlist rtl hdl verilog vhdl logic\$2) adj (stage phase design routine)) ((clock buffer) near4 (skeleton synthesis tree)) ((clock buffer) near2 (tree distribution) near2 (synthes \$7 build\$3 produc\$4 generat\$4 creat\$4))) with ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3)) sta spice)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) with (spec specification configuration requirement definition defin\$3 character \$7 constraint goal) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near (net source domain structure element block need\$4 used utiliz\$7))) And (clock buffer) with (allocat\$4 defin\$5 generat \$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:22
S129	575	((clock buffer) near2 (tree distribution) near2 (synthes \$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:25

S130	246	((clock buffer) near2 (tree distribution) near2 (synthes\$7)) and @ad<"20031128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:31
S131	411	@ad<"20031128" And (netlist (((gate adj level) netlist rtl hdl verilog vhdl logic\$2) adj (stage phase design routine))) sane (((timing time delay slack \$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict \$4)) sta spice\$2)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) with (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribut\$4) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (clock buffer) with (allocat\$4 defin \$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5 budget\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:35
S132	403	@ad<"20031128" And (netlist (((gate adj level) netlist rtl hdl verilog vhdl logic\$2) adj (stage phase design routine))) sane (((timing time delay slack \$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict \$4)) sta spice\$2)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:38

		driven based)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribut\$4 description) or ((identify \$7 determin\$5 calculat\$4 ascertain\$5 list\$3 report \$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (clock buffer) with (allocat\$4 defin \$5 generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5 budget\$4)				
S133	402	@ad<"20031128" And (netlist (((gate adj level) (circuit adj list\$3) rtl hdl verilog vhdl logic\$2) adj (stage phase design routine))) sane (((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat \$5 predict\$4)) sta spice \$2)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribute description propert\$4) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (clock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:43

		apportion\$3 assign\$5 budget\$4)				
S134	414	@ad<"20031128" And (netlist (((gate adj level) (circuit adj list\$3) rtl hdl verilog vhdl logic\$2) adj (stage phase design routine))) sane (((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 simulat\$4 emulat \$5 predict\$4)) sta spice \$2)) And (layout same ((timing near5 (analy\$5 closure converg\$5 verif\$5 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict \$4)) sta spice)) And Delay And Skew\$3 And ((clock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character \$7 constraint goal permission rule attribute description propert\$4) or ((identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3) with (clock near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (clock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5 budget\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 16:46
S135	6752	(((layout ((lay\$3 laid) adj out\$3) ((place\$1 placing placement) near2 (route routing routed))) or ((clock buffer) near4 (skeleton synthesis tree)) ((clock buffer) near2 (tree distribution) near2 (synthes \$7 build\$3 produc\$4 generat\$4 creat\$4))) same ((timing near5 (analy \$5 closure converg\$5 verif \$7 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict \$4 evaluat\$3)) sta spice))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 18:15

S136	1033249	(((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict\$4 evaluat\$3)) sta spice\$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 18:17
S137	172	@ad<"20031128" And (((net schematic (gate adj level) rtl) adj list\$3) netlist\$3) ((gate adj level) (circuit adj list\$3) rtl hdl verilog vhdl logic\$2) adj (cycle stage phase design routine description synthes\$7 specification))) same (((timing time delay slack\$3 skew\$3 transient) near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict\$4 evaluat\$3)) sta spice\$2)) And (((layout ((lay\$3 laid) adj out\$3) ((place\$1 placing placement) near2 (route routing routed))) or ((clock buffer) near4 (skeleton synthesis tree)) ((clock buffer) near2 (tree distribution) near2 (synthes\$7 build\$3 produc\$4 generat\$4 creat\$4))) same ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 driven based simulat\$4 emulat\$5 predict\$4 evaluat\$3)) sta spice)) And Delay And Skew\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 18:22
S138	141	S137 And (layout or (lay adj out)) And ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 static validat\$3 simulat\$4 emulat\$5 predict\$4 evaluat\$3)) sta spice)) And ((clock timing buffer) near10 (spec specification configuration requirement definition defin\$3 character\$7 constraint goal permission rule attribute description propert\$4 (synthesis near (script report))) or ((extract\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 18:23

		identify\$7 determin\$5 calculat\$4 ascertain\$5 list \$3 report\$3 specify\$3 (synthesis near (script report))) with ((clock\$3 clk buffer\$3) near6 (net path source domain structure element block need\$4 used utiliz\$7 component))) And (clock buffer) with (allocat\$4 define defining generat\$5 distribut\$3 allot\$5 appropriat\$3 earmark\$3 apportion\$3 assign\$5 budget\$4 specify\$)				
S141	68	@ad<"20031128" and (layout (post adj layout)) with ((timing near5 (analy \$5 closure converg\$5 verif \$7 optim\$7 check\$4 validat \$3)) sta spice) and ((correct\$3 optim\$7 refin \$3 refinement resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning) with (skew))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 20:57
S142	10	S141 and ((correct\$3 optim \$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress\$3 remed \$4 modif\$7 repair\$3 reshap \$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning dimensioning) with delay) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 delay with (output\$4 launch))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 20:58

S143	12	S141 and ((correct\$3 optim\$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug\$5 modulat\$3 tune tuning dimensioning) with delay) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 (delay buffer repeater) with (output\$4 launch))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 20:59
S144	35	S141 and ((correct\$3 optim\$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug\$5 modulat\$3 tune tuning dimensioning) with delay) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 (delay buffer repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 21:27
S146	312	(delay near2 violation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:27
S147	31	@ad< "20031128" and ((clock buffer) with tree) with ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 validat\$3)) sta spice) and ((correct\$3 optim\$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif\$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug\$5 modulat\$3 tune tuning)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:29

		with (skew))				
S149	23	@ad< "20031128" and (((clock buffer) with tree) or cts bct) with ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 validat\$3)) sta spice) and ((correct\$3 optim\$7 refin\$3 refinement resolv\$3 fix\$3 adjust\$4 chang\$4 revis\$3 amend\$4 rectif\$7 redress \$3 remed\$4 modif\$7 repair \$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz \$5 debug\$5 modulat\$3 tune tuning) with (skew)) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost\$4 plug\$4 supplement\$3) near4 (delay buffer repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:31
S148	20	@ad< "20031128" and ((clock buffer) with tree) with ((timing near5 (analy \$5 closure converg\$5 verif \$7 optim\$7 check\$4 validat \$3)) sta spice) and ((correct\$3 optim\$7 refin \$3 refinement resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning) with (skew)) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost \$4 plug\$4 supplement\$3) near4 (delay buffer repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:31

S150	65	@ad<"20031128" and (((clock buffer) with tree) or cts bct) with ((timing near5 (analy\$5 closure converg\$5 verif\$7 optim\$7 check\$4 validat\$3)) sta spice optim\$7) and ((correct\$3 optim\$7 refin \$3 refinement resolv\$3 fix \$3 adjust\$4 chang\$4 revis \$3 amend\$4 rectif\$7 redress\$3 remed\$4 modif \$7 repair\$3 reshap\$3 compensat\$3 enhanc\$5 reduc\$5 alter\$3 alteration reconstruct\$3 improv\$5 drc reparametriz\$5 debug \$5 modulat\$3 tune tuning) with (skew)) and ((add\$4 insert\$3 implement\$3 appenend\$3 affix\$3 boost \$4 plug\$4 supplement\$3) near4 (delay buffer repeater))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/08 22:32
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